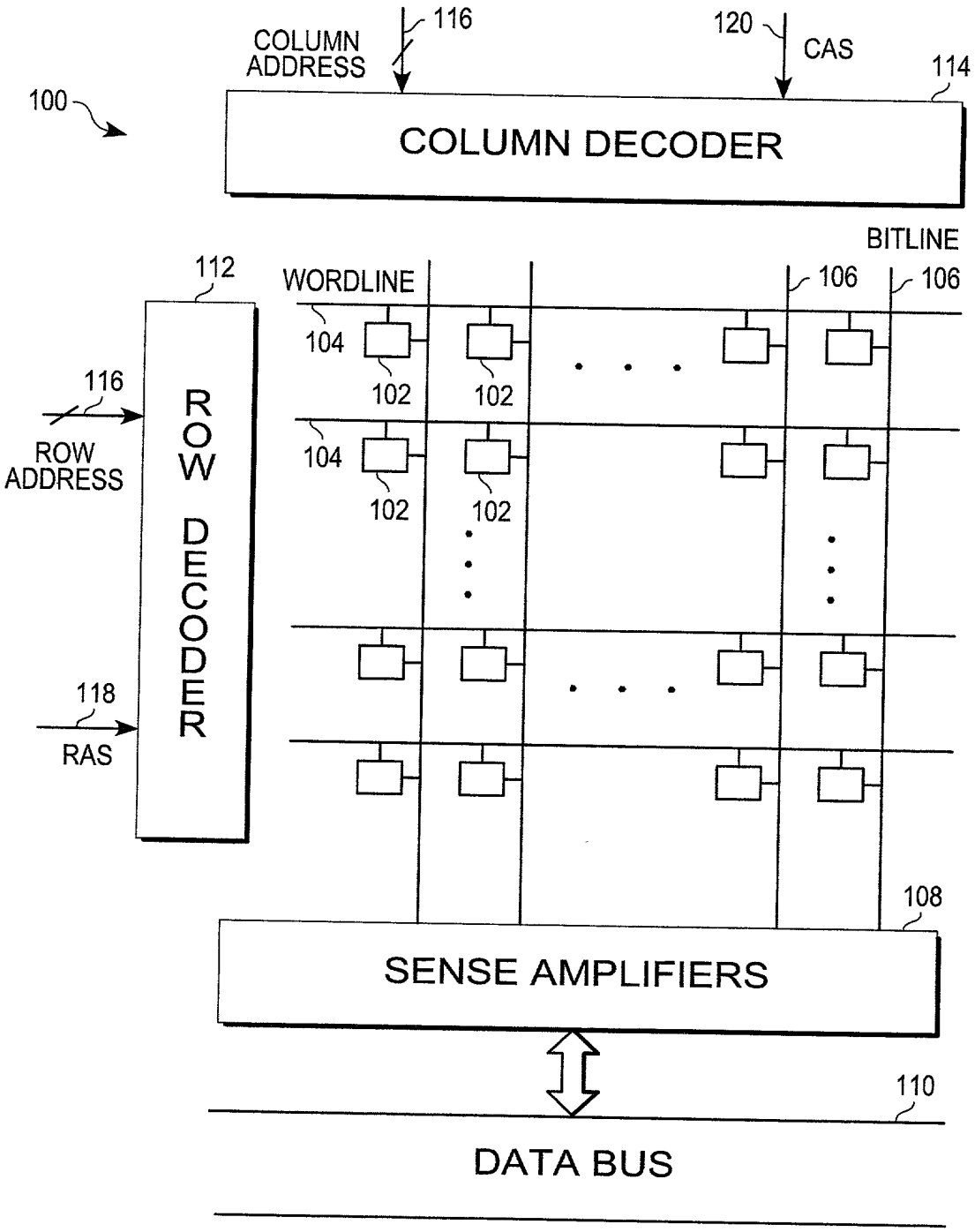
COLUMN ADDRESS
116
120
CAS
114
100
COLUMN DECODER
BITLINE
112
WORDLINE
106
106
104
102
102
104
102
102
116
ROW ADDRESS
ROW DECODER
118
RAS
108
SENSE AMPLIFIERS
110
DATA BUS

*Fig. 1*

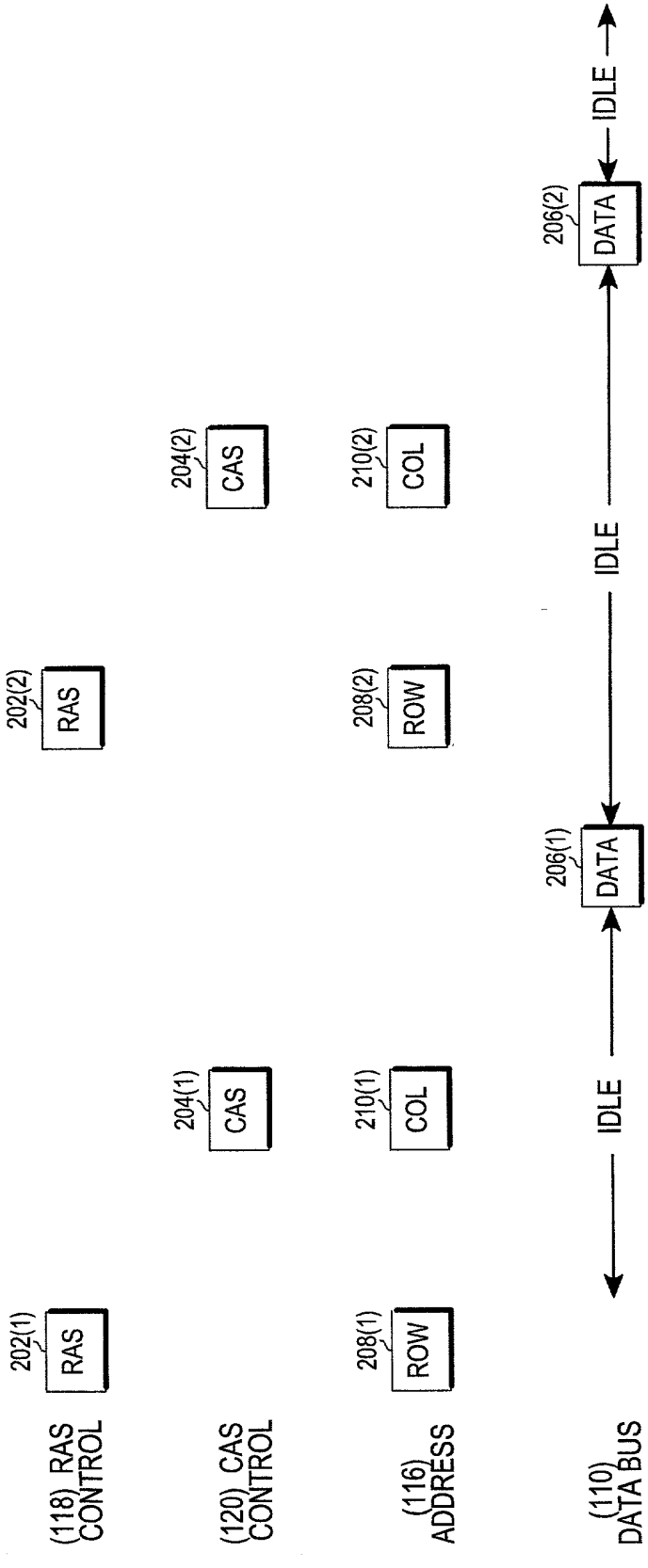
(118) RAS CONTROL
(120) CAS CONTROL
(116) ADDRESS
(110) DATA BUS
202(1) RAS
204(1) CAS
208(1) ROW
210(1) COL
206(1) DATA
IDLE
202(2) RAS
204(2) CAS
208(2) ROW
210(2) COL
206(2) DATA
IDLE

Fig. 2

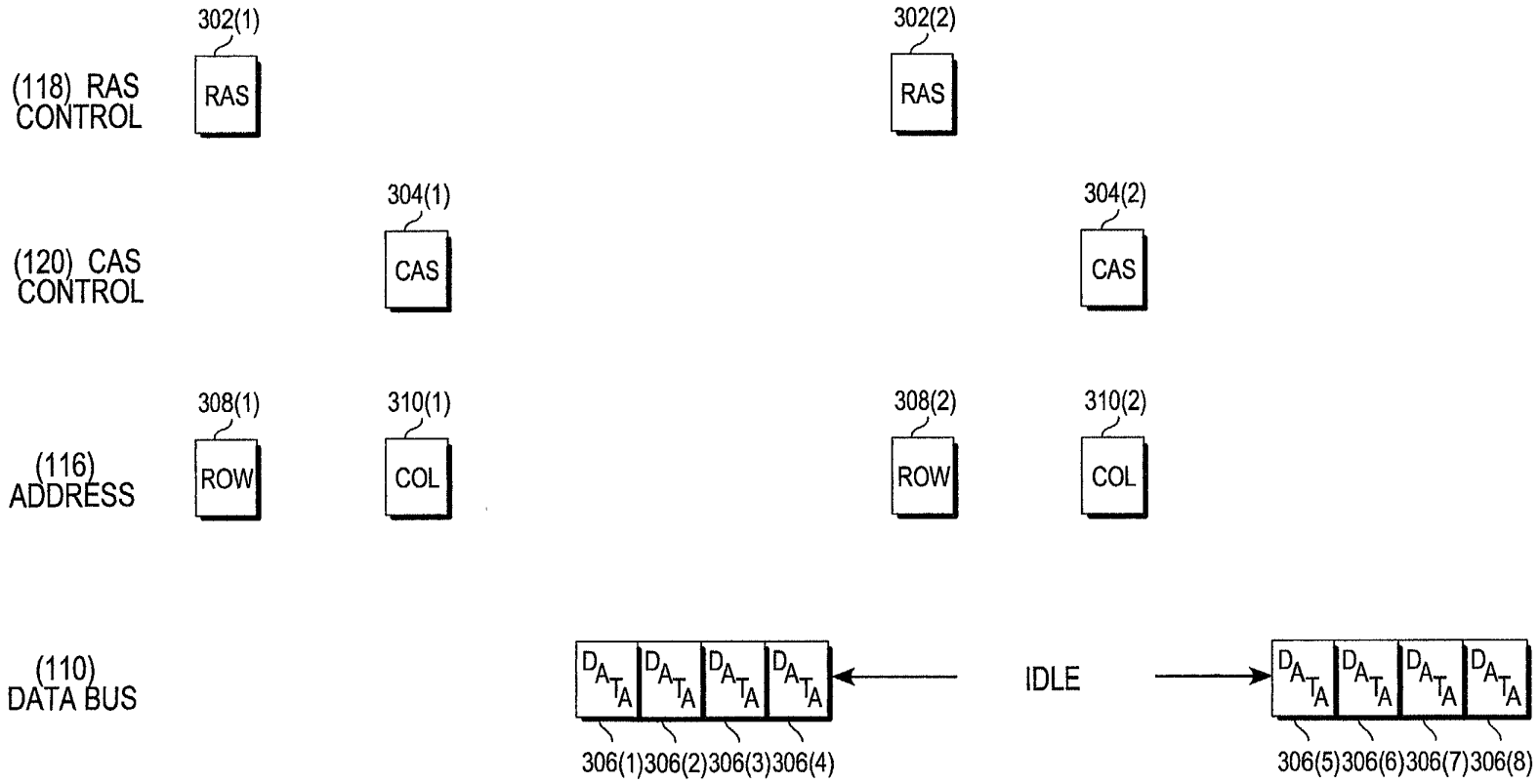
302(1)
302(2)
(118) RAS CONTROL
RAS
RAS
304(1)
304(2)
(120) CAS CONTROL
CAS
CAS
308(1)
310(1)
308(2)
310(2)
(116) ADDRESS
ROW
COL
ROW
COL
(110) DATA BUS
DATA
DATA
DATA
DATA
IDLE
DATA
DATA
DATA
DATA
306(1)306(2)306(3)306(4)
306(5)306(6)306(7)306(8)

*Fig. 3*

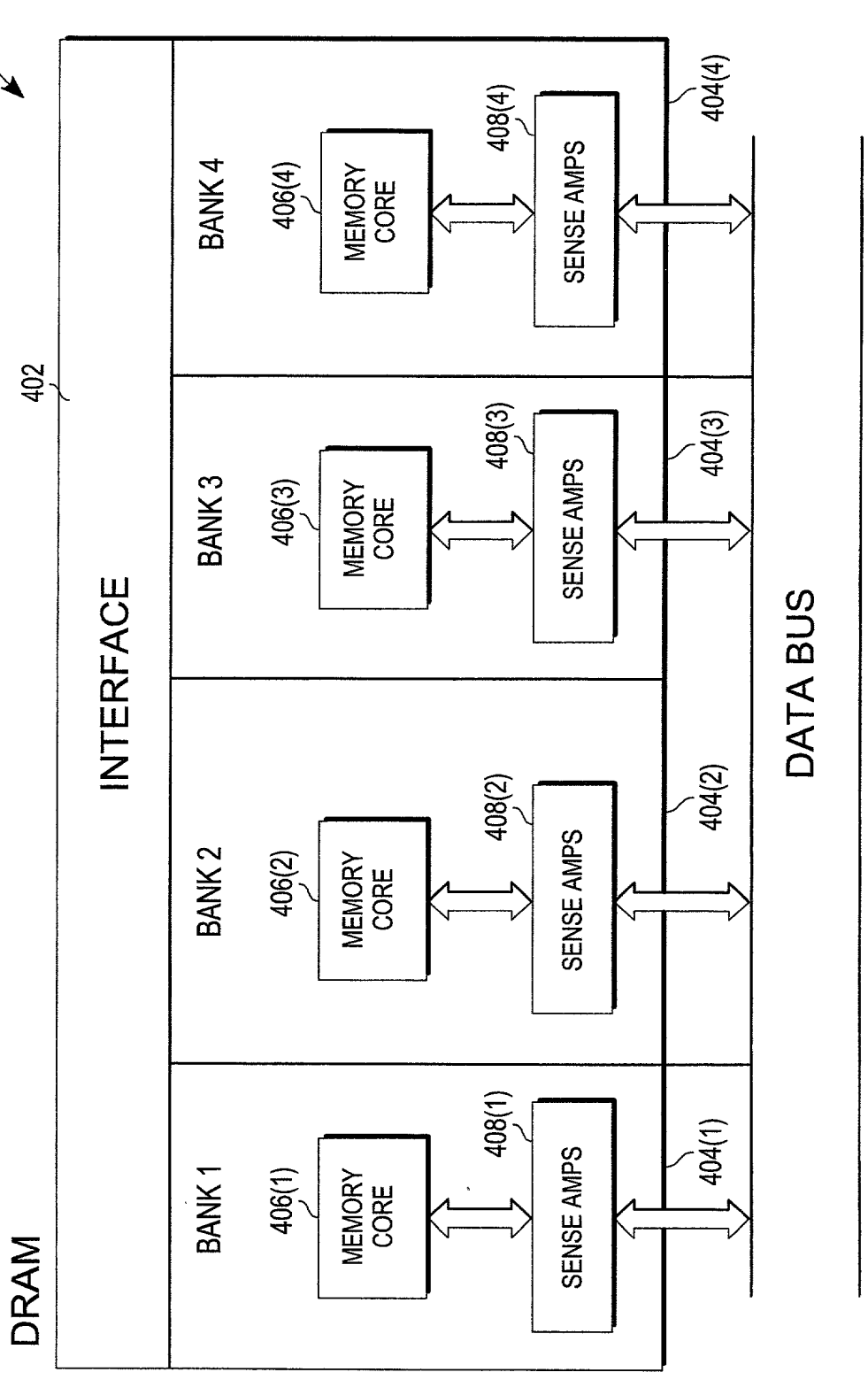
400
DRAM
INTERFACE
402
BANK 1
BANK 2
BANK 3
BANK 4
406(1)
406(2)
406(3)
406(4)
MEMORY CORE
408(1)
408(2)
408(3)
408(4)
SENSE AMPS
404(1)
404(2)
404(3)
404(4)
DATA BUS

Fig. 4

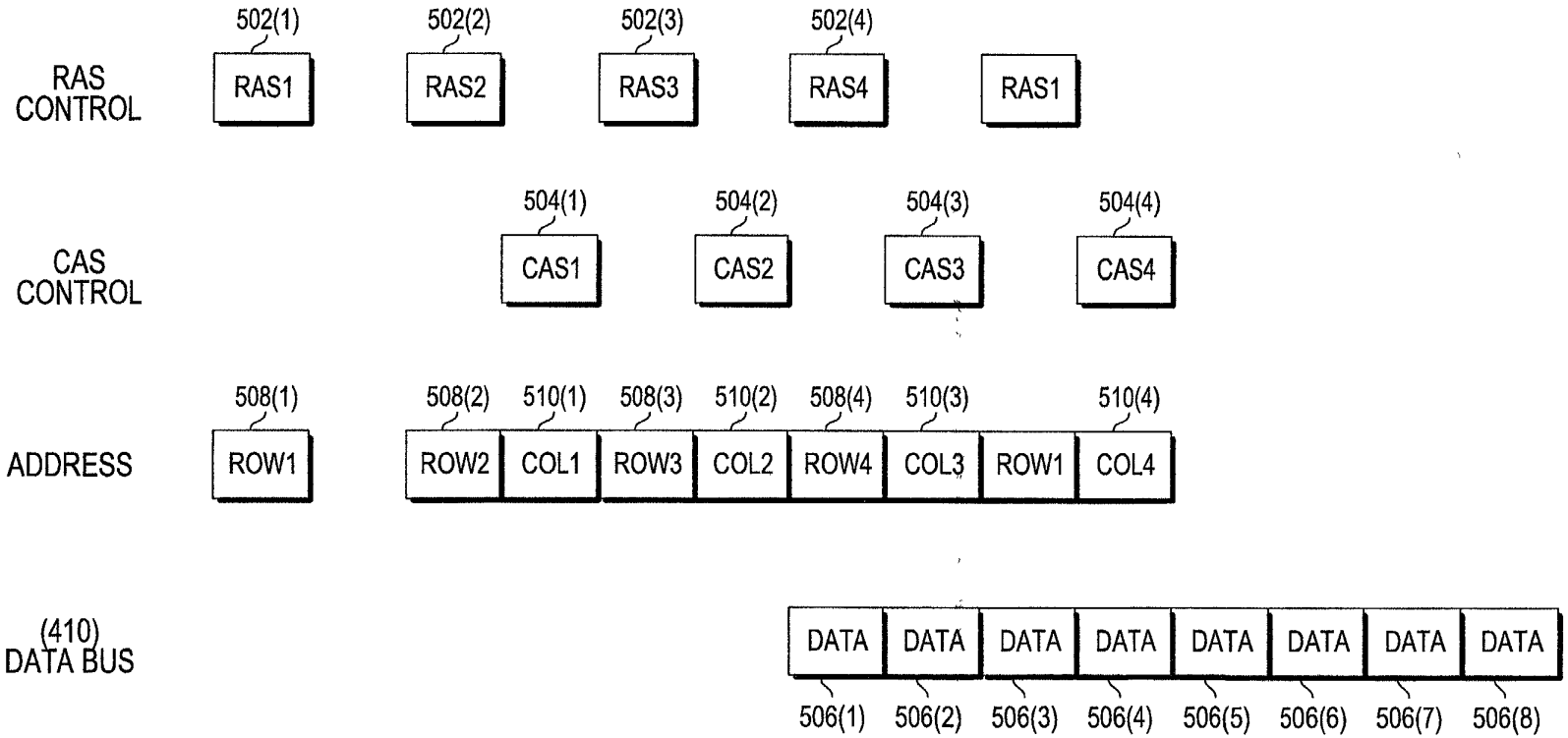
RAS CONTROL
502(1)
RAS1
502(2)
RAS2
502(3)
RAS3
502(4)
RAS4
RAS1
CAS CONTROL
504(1)
CAS1
504(2)
CAS2
504(3)
CAS3
504(4)
CAS4
ADDRESS
508(1)
ROW1
508(2)
ROW2
510(1)
COL1
508(3)
ROW3
510(2)
COL2
508(4)
ROW4
510(3)
COL3
ROW1
510(4)
COL4
(410)
DATA BUS
DATA
506(1)
506(2)
506(3)
506(4)
506(5)
506(6)
506(7)
506(8)

*Fig. 5*

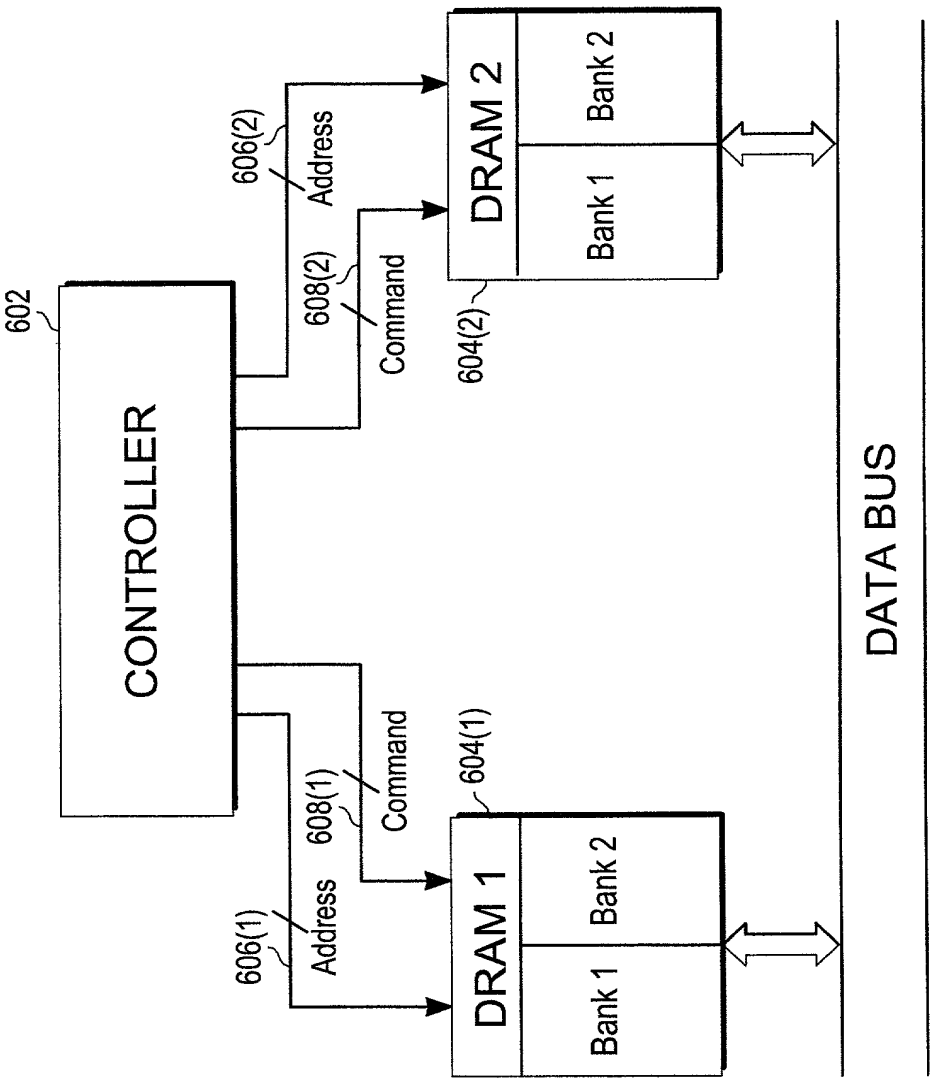
602
CONTROLLER
606(1)
Address
608(1)
Command
606(2)
Address
608(2)
Command
604(1)
DRAM 1
Bank 1
Bank 2
604(2)
DRAM 2
Bank 1
Bank 2
DATA BUS

Fig. 6

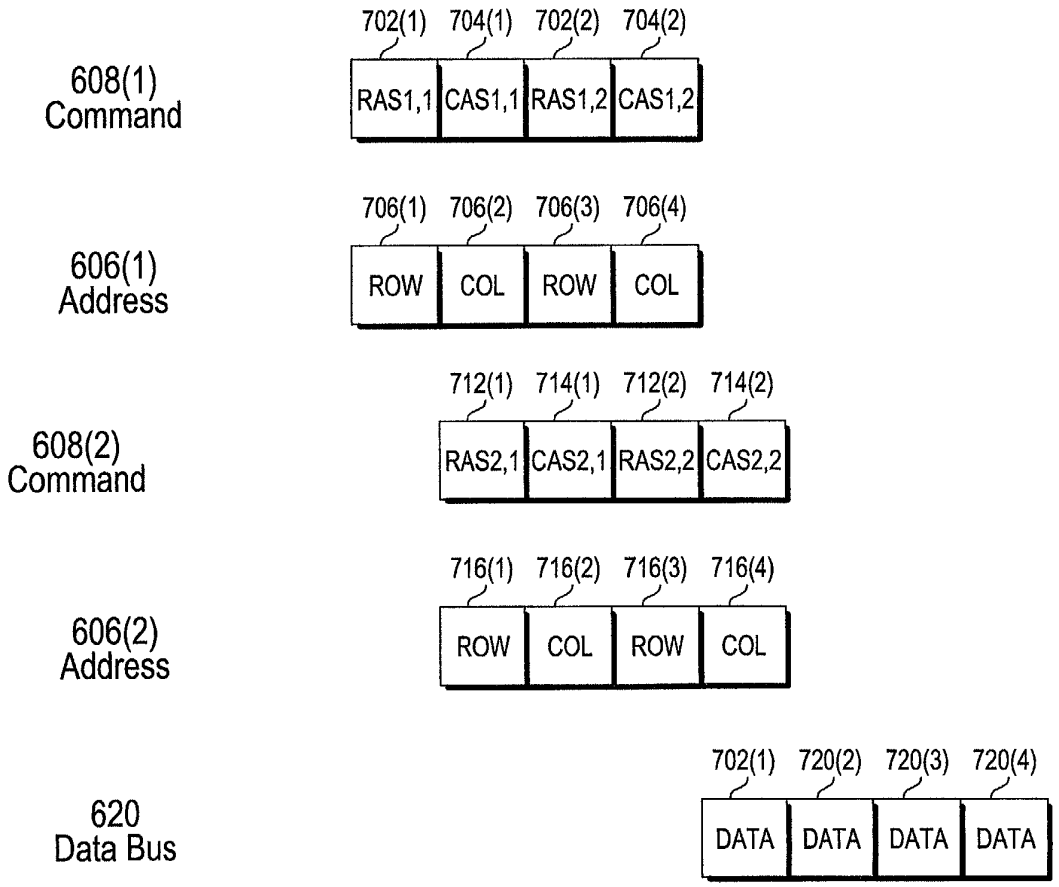
608(1) Command
702(1)
704(1)
702(2)
704(2)
RAS1,1
CAS1,1
RAS1,2
CAS1,2
606(1) Address
706(1)
706(2)
706(3)
706(4)
ROW
COL
ROW
COL
608(2) Command
712(1)
714(1)
712(2)
714(2)
RAS2,1
CAS2,1
RAS2,2
CAS2,2
606(2) Address
716(1)
716(2)
716(3)
716(4)
ROW
COL
ROW
COL
620 Data Bus
702(1)
720(2)
720(3)
720(4)
DATA
DATA
DATA
DATA

*Fig. 7*

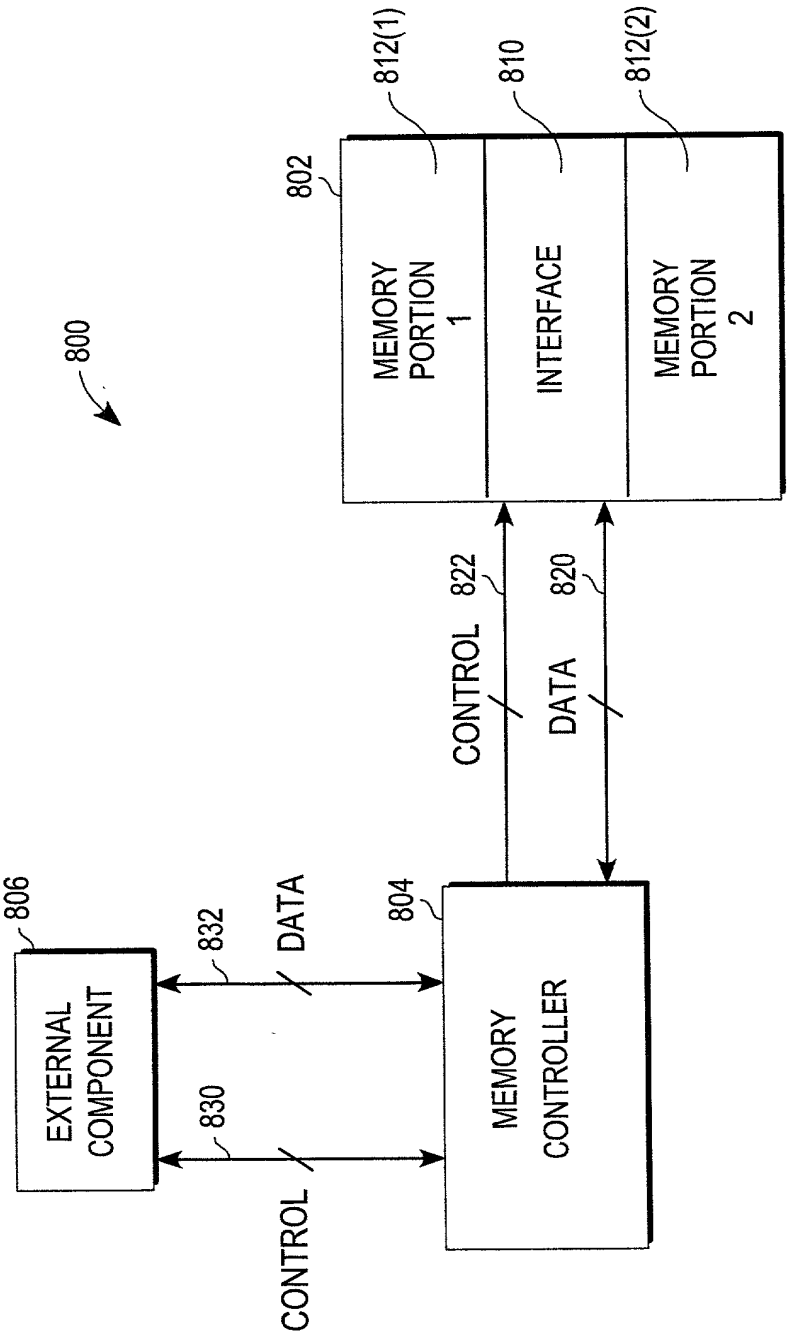
800
802
812(1)
810
812(2)
MEMORY PORTION 1
INTERFACE
MEMORY PORTION 2
822
820
CONTROL
DATA
804
806
832
DATA
830
CONTROL
EXTERNAL COMPONENT
MEMORY CONTROLLER

Fig. 8

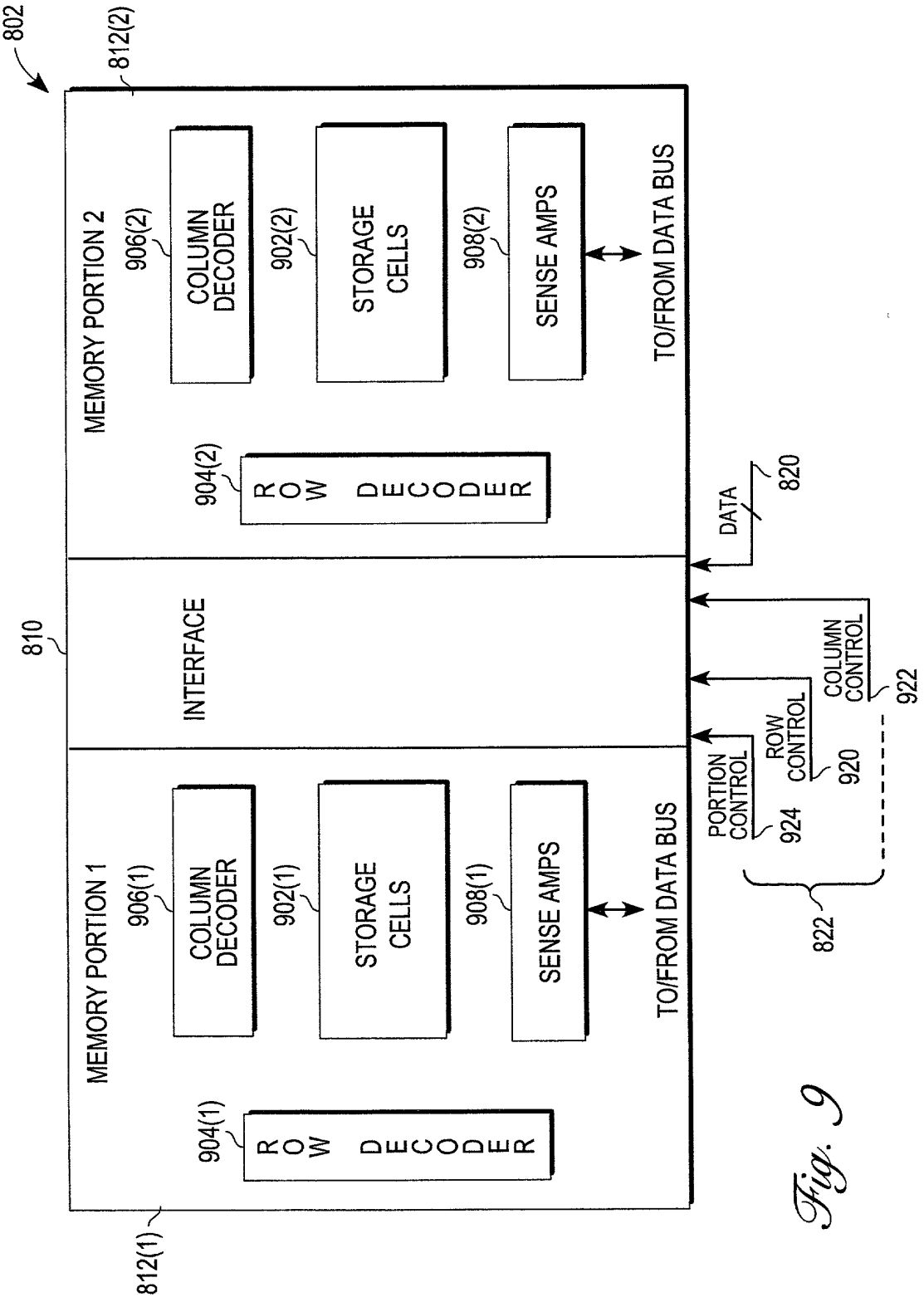
802
812(2)
MEMORY PORTION 2
906(2)
COLUMN DECODER
902(2)
STORAGE CELLS
908(2)
SENSE AMPS
TO/FROM DATA BUS
904(2)
ROW DECODER
DATA
820
810
INTERFACE
MEMORY PORTION 1
906(1)
COLUMN DECODER
902(1)
STORAGE CELLS
908(1)
SENSE AMPS
TO/FROM DATA BUS
PORTION CONTROL
924
ROW CONTROL
920
COLUMN CONTROL
922
904(1)
ROW DECODER
822
812(1)

Fig. 9

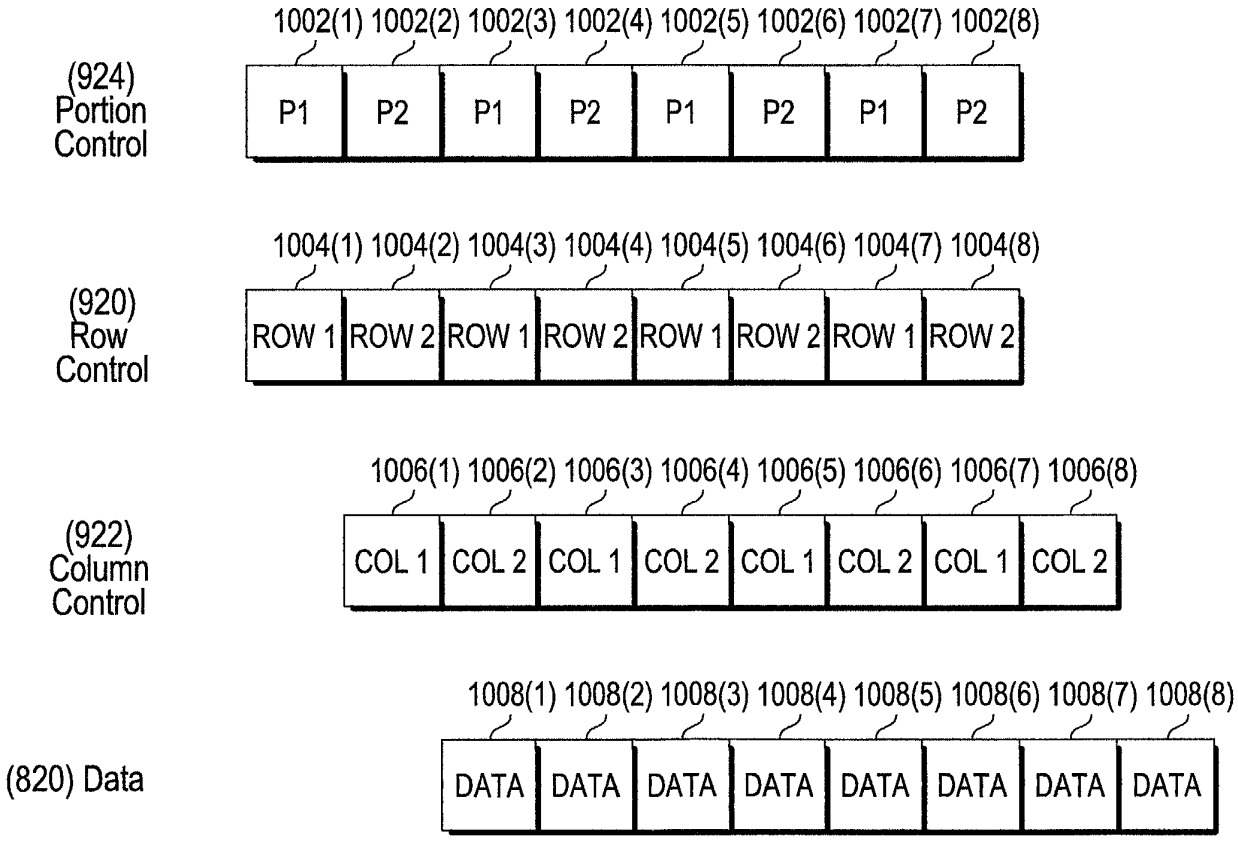
1002(1) 1002(2) 1002(3) 1002(4) 1002(5) 1002(6) 1002(7) 1002(8)
(924) Portion Control
P1 P2 P1 P2 P1 P2 P1 P2
1004(1) 1004(2) 1004(3) 1004(4) 1004(5) 1004(6) 1004(7) 1004(8)
(920) Row Control
ROW 1 ROW 2 ROW 1 ROW 2 ROW 1 ROW 2 ROW 1 ROW 2
1006(1) 1006(2) 1006(3) 1006(4) 1006(5) 1006(6) 1006(7) 1006(8)
(922) Column Control
COL 1 COL 2 COL 1 COL 2 COL 1 COL 2 COL 1 COL 2
1008(1) 1008(2) 1008(3) 1008(4) 1008(5) 1008(6) 1008(7) 1008(8)
(820) Data
DATA DATA DATA DATA DATA DATA DATA DATA

*Fig. 10*

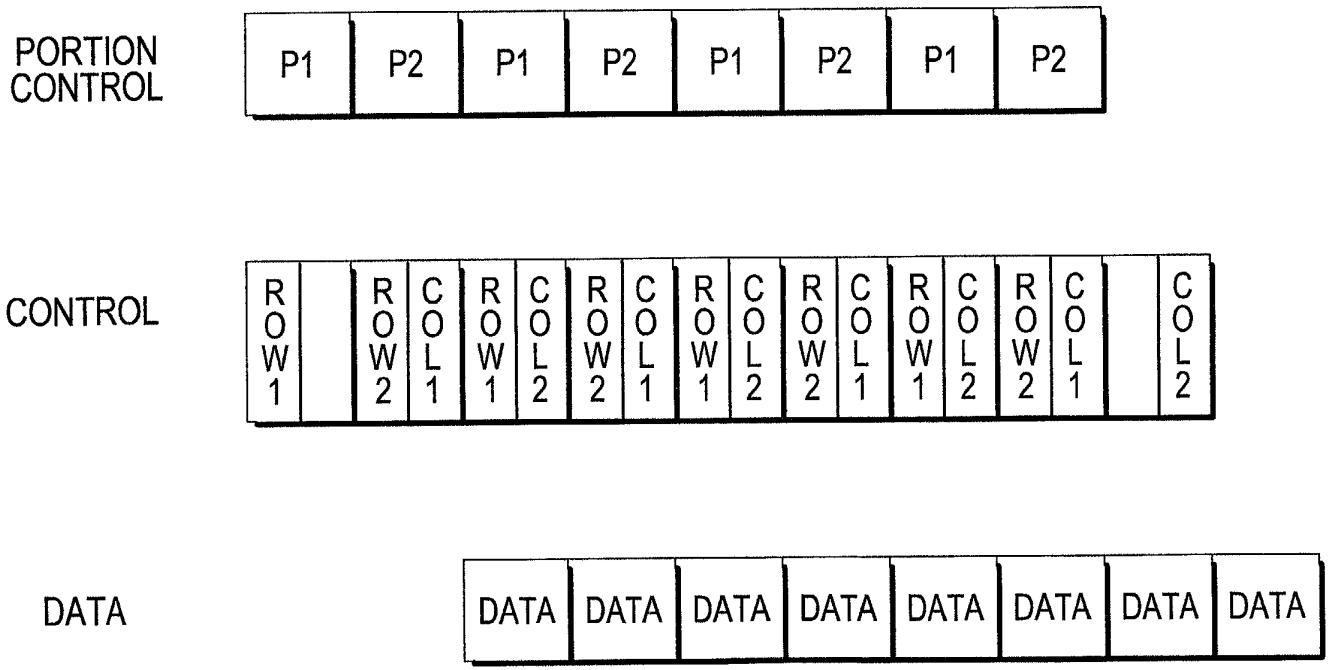
PORTION CONTROL
P1
P2
P1
P2
P1
P2
P1
P2
CONTROL
ROW1
ROW2
COL1
ROW1
COL2
ROW2
COL1
ROW1
COL2
ROW2
COL1
ROW1
COL2
ROW2
COL1
COL2
DATA
DATA
DATA
DATA
DATA
DATA
DATA
DATA
DATA

*Fig. 11*

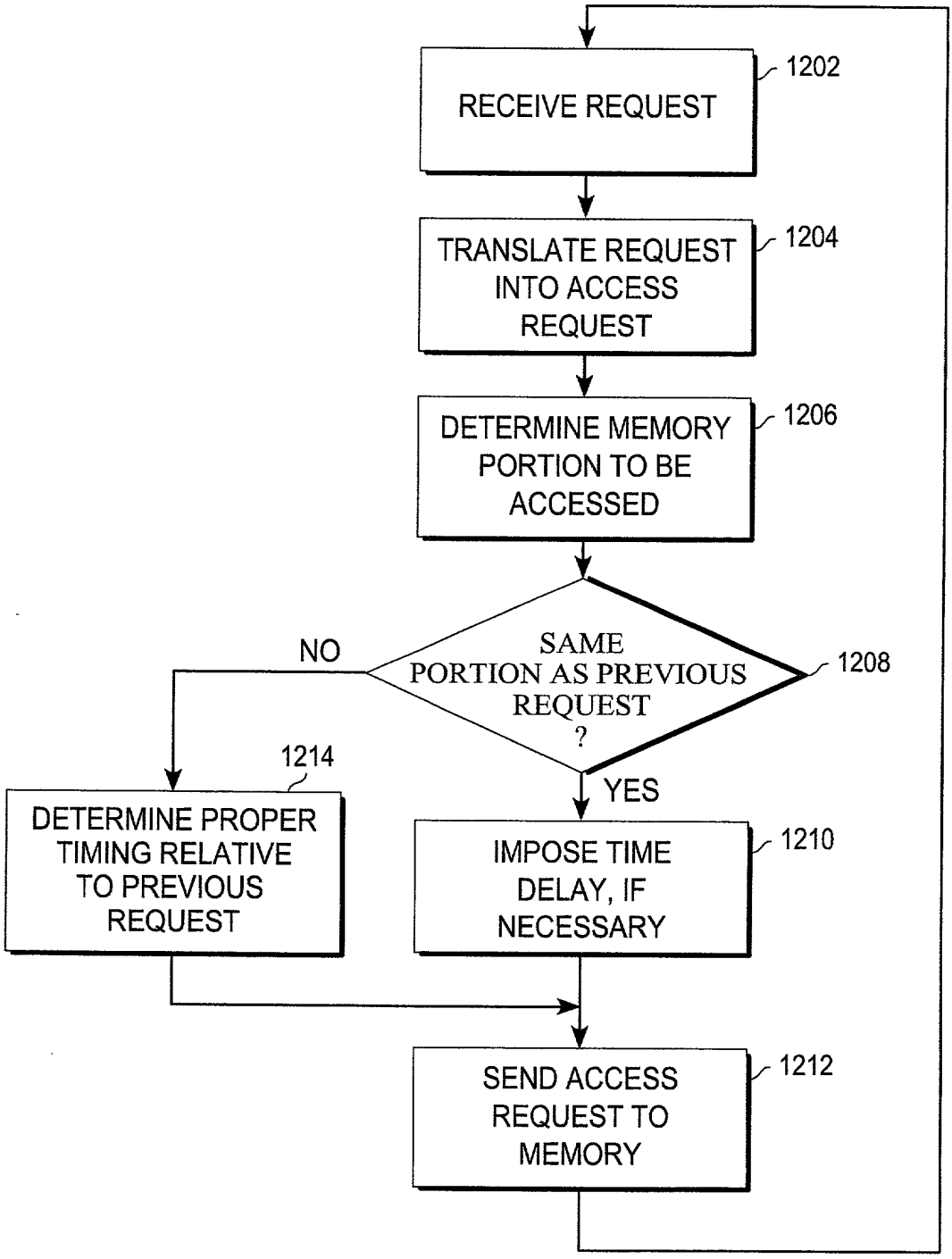
RECEIVE REQUEST
1202
TRANSLATE REQUEST INTO ACCESS REQUEST
1204
DETERMINE MEMORY PORTION TO BE ACCESSED
1206
SAME PORTION AS PREVIOUS REQUEST ?
1208
NO
YES
DETERMINE PROPER TIMING RELATIVE TO PREVIOUS REQUEST
1214
IMPOSE TIME DELAY, IF NECESSARY
1210
SEND ACCESS REQUEST TO MEMORY
1212

*Fig. 12*